Yee-Chia YEO

Ph.D (University of California, Berkeley)

Assistant Professor
Department of Electrical & Computer Engineering
National University of Singapore
4 Engineering Drive 3
Singapore 117576

Phone: 65-6874 2298
E-mail : eleyeoyc@nus.edu.sg

MAJOR RESEARCH INTERESTS

Research in my group concentrates on nanoelectronics and semiconductor nanotechnology. We actively engage the challenges faced in the miniaturization of electronics circuits and semiconductor devices. Recently, we focus on the fabrication and characterization of nanoscale transistors, on strain engineering techniques to enhance the performance of nanoscale devices, and on materials innovation to improve transistor performance. Work in this area has direct impact on the future of electronics products and semiconductor technology. Current projects in our group include

1. Nanoelectronics. Nanoscale transistor fabrication and characterization.
2. Strain and band structure engineering in solid-state devices.
3. Novel materials for nanotechnology.

RECENT REPRESENTATIVE PUBLICATIONS

1. Y. C. Yeo, M. F. Li, T. C. Chong, and P. Y. Yu, "Theoretical study of the energy band structure of partially CuPt-ordered $Ga_{0.5}In_{0.5}P$", *Physical Review B*, vol. 55, no. 24, pp. 16414-16419, Jun 1997.
2. Y. C. Yeo, T. C. Chong, and M. F. Li, "Electronic band structures and effective-mass parameters of wurtzite GaN and InN", *J. Applied Physics*, vol. 83, no. 3, pp. 1429-1436, Feb 1998.
3. Y. C. Yeo, V. Subramanian, J. Kedzierski, P. Xuan, T.-J. King, J. Bokor, and C. Hu, "Nanoscale ultra-thin-body silicon-on-insulator P-MOSFET with a SiGe/Si heterostructure channel", *IEEE Electron Device Letters*, vol. 21, no. 4, pp. 161-163, Apr 2000.
4. Y.-C. Yeo, Q. Lu, P. Ranade, H. Takeuchi, K. J. Yang, I. Polishchuk, T.-J. King, C. Hu, S. C. Song, H. F. Luan, and D.-L. Kwong, "Dual-metal gate CMOS technology with ultra-thin silicon nitride gate dielectric", *IEEE Electron Device Letters*, vol. 22, no. 5, pp. 227-229, May 2001.
5. (Invited Review) Y.-C. Yeo, Q. Lu, and C. Hu, "Gate Oxide Reliability: Anode Hole Injection Model and its Applications", *International J. High Speed Electronics and Systems*, vol. 11, no. 3, pp. 849-886, 2001.
6. (IEEE Paul Rappaport Award) Y.-C. Yeo, V. Subramanian, J. Kedzierski, P. Xuan, T.-J. King, J. Bokor, and C. Hu, "Design and fabrication of 50 nm thin-body P-MOSFETs with a silicon-germanium heterostructure channel", *IEEE Trans. Electron Devices*, vol. 49, no. 2, pp. 279-286, Feb. 2002.
7. Y.-C. Yeo, T.-J. King, and C. Hu, "Metal-dielectric band alignment and its implications for metal gate CMOS technology", *J. Applied Physics*, vol. 92, no. 12, pp. 7266-7271, Dec. 2002.
8. Y.-C. Yeo, T.-J. King, and C. Hu, "Direct tunneling gate leakage and scalability of alternative gate dielectrics", *Applied Physics Letters*, vol. 81, no. 11, pp. 2091-2093, Sep. 2002.
9. Y.-C. Yeo, T.-J. King, and C. Hu, "MOSFET gate leakage modeling and selection guide for alternative gate dielectrics based on leakage considerations", *IEEE Trans. Electron Devices*, vol. 50, pp. 1027-1035, Apr. 2003.
10. (Invited Paper) Y.-C. Yeo, "Metal gate technology for nanoscale transistors- Material selection and integration issues", presented at *International Conference on Materials for Advanced Technologies*, Singapore, Dec. 2003.
11. (Invited Paper) Y.-C. Yeo, "Enhancing CMOS transistor performance using lattice-mismatched materials in source/drain regions," *3rd International SiGe Technology and Device Meeting*, Princeton, NJ, May 15-17, 2006, pp. 264-265; *Semiconductor Science and Technology*, vol. 22, pp. S177-S182, Jan. 2007.
12. (Invited Paper) Y.-C. Yeo, "Silicon-Carbon Source/Drain: Selective epitaxy, process integration, and transistor strain engineering," *2006 Silicon-Germanium Materials, Processing, and Devices Symposium, 210th Electrochemical Society Meeting*, Cancun, Mexico, Oct. 29 - Nov. 3, 2006, pp. 1143-1150.